REMARKS/ARGUMENTS

Claims 1, 8, 10, and 11 are rejected under 35 U.S.C. 102(b) as being unpatentable over by Cucchi (US 4,899,352) in view of Riou (US 5,649,146).

Response:

Claims 1, 2, 8-10, 12, and 13 have been amended to remove intended use language from the claims. No new matter has been added through the amendments to these claims, and acceptance of the amended claims is respectfully requested.

Furthermore, the applicant respectfully submits that the combination of Cucchi and Riou does not teach all of the features of independent claims 1, 8, 10, 12, and 13. Specifically, the references do not teach the claimed features of the write blocking logic comprising a write select counter and a read select counter as claimed.

Each of these claims recites the features of "a write select counter electrically connected to the first counter counting how many data the configurable write buffer has ever stored and generating a write select value" and "a read select counter electrically connected to the first counter counting how many data the configurable write buffer has ever transferred to the single port memory unit and generating a read select value".

The Examiner has relied upon Riou for teaching the write blocking logic containing the write select counter and the read select counter. Riou discloses in columns 1-4 a modular addressing buffer, which is also known as a circular buffer. Riou teaches in Figures 1 and 2 that a moving pointer 16, 33 is used to point to the current address being read.

Riou also teaches an improved circular buffer which can have a buffer of

any size and start at any location in memory. Riou discloses in column 4, lines 4-33 a circuit for incrementing a current access address of a circular buffer. Riou teaches in column 4, lines 24-28 that the circuit considers the current address, the increment value, and the limit address when making its decisions about what the increment address will be.

However, despite the above, Riou does not teach counting how many data the configurable write buffer has ever stored and generating a write select value. Similarly, Riou does not teach counting how many data the configurable write buffer has ever transferred to the single port memory unit and generating a read select value. The only pointer that Riou teaches is the pointer of the current access address. There is no mention of a separate write address pointer and a read access pointer as the Examiner has stated Riou teaches. Therefore, the applicant respectfully submits that Riou fails to teach the write select counter and read select counter recited in independent claims 1, 8, 10, 12, and 13.

Since the combination of Cucchi and Riou fails to teach all of the limitations of claims 1, 8, 10, 12, and 13, these claims are patentable over the cited prior art. Claims 2-7 and 9 are dependent on claims 1 and 8 and should be allowed if their respective base claims are allowed. Reconsideration of claims 1-10, 12, and 13 is therefore respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu

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Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)